
Master's thesis position:

Implementation and Test of a High-Resolution Time-to-Digital Converter



Goal:

- Software implementation of a high-resolution Time-to-Digital Converter (TDC), based on field programmable gate arrays (FPGAs).
- Software implementation of data transfer interface between the FPGA-development board and a PC via PCIe, Ethernet and USB

Requirements:

- C++ programming skills
- Experience in programming with VHDL beneficial
- Experience in programming of Virtex or Spartan FPGA boards (Xilinx) beneficial

Description:

For a project in quantum key distribution, we are developing a single photon detection system with the necessity of accurate measurement of the arrival times of the photons. In this context, we have implemented an FPGA based solution.

FPGAs consist of many carry lines that connect basic logic elements. Those lines are used to implement mathematical functions such as comparators, counters etc. The timing delay of each element lies in the order of several 10 ps and can be considered as constant under certain conditions. Therefore, those carry lines can be used as delay elements for a time to digital converter. However, achieving a high resolution of a TDC is only one part of a successful implementation. For a real-time analysis, the timing of detected signals should be rapidly transferred to a PC and processed.

The main task of the thesis will be the improvement of the existing TDC. To increase performance, the existing system shall be migrated to a new FPGA board and communication interfaces should be implemented. Hereby, a comparison between the existing FPGA based TDC solutions has to be carried out and improvement schemes should be defined and implemented. Subsequently, the system should be tested.

Suggested Beginn:

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Contact:

Oleg Nikiforov oleg.nikiforov@physik.tu-darmstadt.de

Web: <http://www.iap.tu-darmstadt.de/lqo>
<https://www.crossing.tu-darmstadt.de>

